Abstract

A method and a jitter buffer regulating circuit for regulating a jitter buffer

Transmission delays due to the buffering (d_p) of data packets (DP1, DP2, DP3) are registered for the purpose of regulating a jitter buffer (JP). Weighted mean delay values (d_l) are continuously derived from registered transmission delays (d_p), with a shorter transmission delay receiving a higher weighting than a longer transmission delay. A read-out speed (CLK) of the jitter buffer (JP) is then regulated as a function of the continuously derived weighted mean delay values (d_l) in such a way that the weighted mean delay values (d_l) are adjusted as a regulating variable to a predefined desired delay (sd_l).

Figure 2